Product Introduction

GALT61120

Automotive Headlight Matrix LED lighting Controller IC

2024.12

1 Product Characteristics

Memory and interface

- Expandable EEPROM

Clock

- External clock, providing 8MHz or 16MHz clock

Power supply

- Input voltage range: 4.5 V~ 60 V

12 integrated bypass switches

- 12 channels, 4 groups, 3 series switches
- Single-channel low on-resistance ($R_{DS(on)}$), 120mΩ
- Maximum cross-switching voltage: 40V
- Maximum switch-to-ground voltage: 70V

Communication peripherals

- Multi-drop UART communication interface. Up to 31 addressable devices, compatible with the CAN physical layer, with a minimum number of wires in the cable harness
- I2C for connecting an external EEPROM

Analog peripherals

- 2 8-bit ADCs with multiplexer input

Timer

- Communication watchdog timer

Programmable 10-bit PWM dimming

- Single phase shift and pulse width
- Device synchronization

CRC computing unit

LED open / short detection and protection

ESD

- Automotive AEC-Q100 Grade1: Operating temperature range -40℃ to 125℃
- HBM=±8000V
- CDM=±2000V

Package

- E-TQFP48

Applications

- Automotive headlight system
- High brightness LED matrix system
- ADB or glare-free high beam
- Sequential turn and animated daytime running lights

Contents

2 Introduction

GALT61120 is an automotive headlight matrix LED lighting controller IC, which integrates 12 60V high-voltage switch MOSFETs, 4 groups of 3 series high-voltage switches, and each switch supports a maximum current of 1.5A; The single pixel LED is controlled independently to realize the full dynamic adaptive lighting, which is suitable for the application scenario of automotive light ADB.

GALT61120 is compatible with CAN physical layer through a multi-drop UART interface, with a maximum communication rate of 1Mbps. It supports cascading of up to 32 chips. The I2C can connect to an external EEPROM for read and write operations. The EEPROM is used to store system calibration data.

The ADC has two multiplexers to collect and measure NTC, which is used as system temperature compensation and overtemperature protection, and measures the LED binning to achieve the overall consistency of LED brightness.

The internal charge pump rail provides gate drive voltage for LED bypass switches. To reduce conduction losses and power consumption, the bypass switches use low on-resistance ($R_{DS(on)}$: 120mΩ).

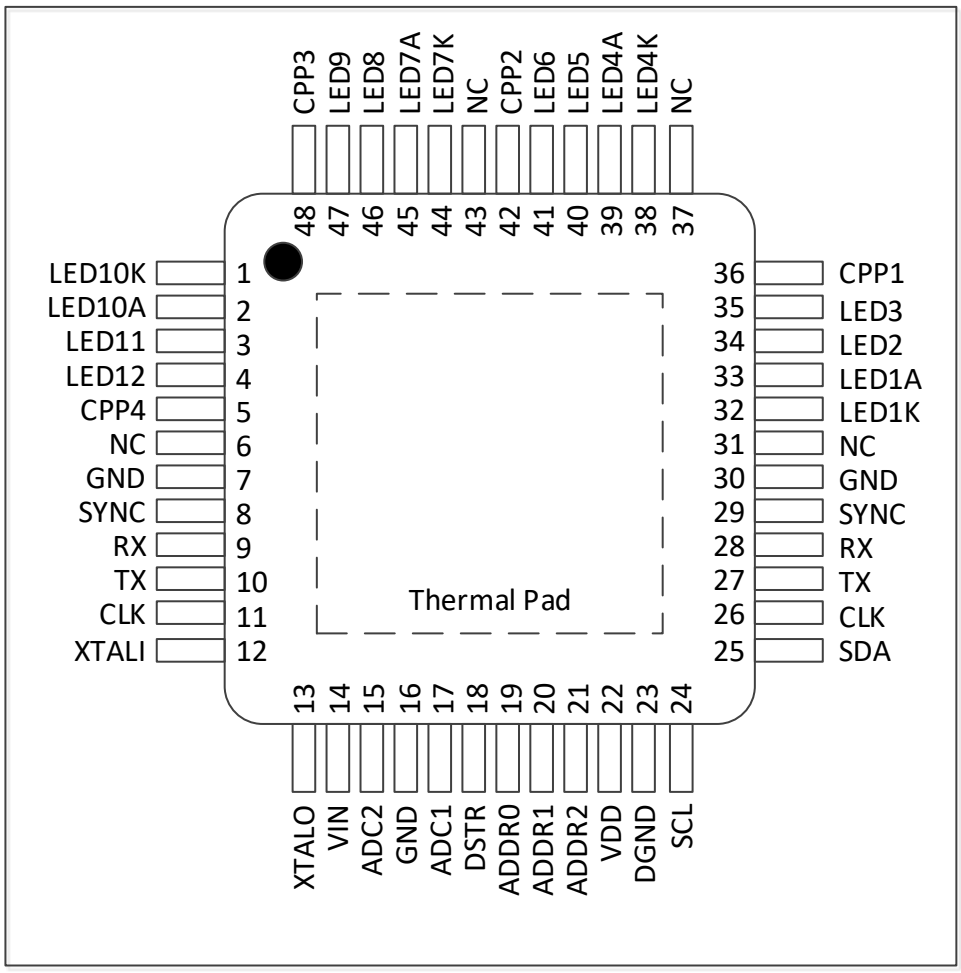
The phase shift and pulse width of individual LED in the string can be adjusted by software programming, and the PWM frequency can be adjusted by internal registers to synchronize multiple devices. During PWM dimming, the slew rate of the switches is programmable, and adjusting the slew rate can help mitigate EMI concerns.

The chip incorporates an open LED protection function through programmable thresholds. It can detect LED open or short circuits and provide feedback through the serial interface.

3 Pin Information

3.1 Pin distribution

Figure 1 GALT61120 Pin Distribution Diagram



3.2 Pin function description

Table 1 Abbreviations and Define Used in Pin Function Description Table

Name	Abbreviation	Definition
Pin name	Pin name	
Pin type	I	Only input pin
	O	Only output pin
	I/O	Input / output
	G	Ground pin
	NC	No connection

Name	Abbreviation	Definition
	AI	Analog input
	AO	Analog output

Table 2 GALT61120 Pin Function Description

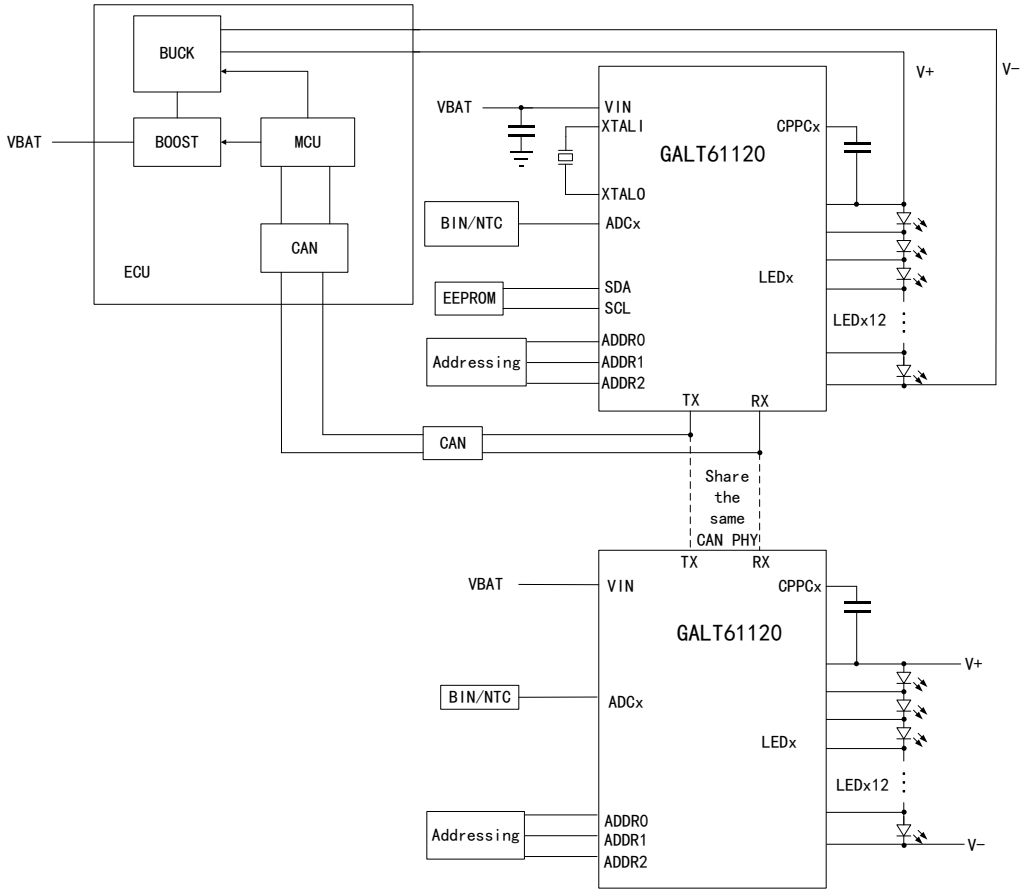
E-TQFP	Name	Type	Function
-	Thermal Pad	G	Connects to system ground.
1	LED10K	I/O	Connects to the cathode of LED10.
2	LED10A	I/O	Connects to the cathode of LED11 and the anode of LED10.
3	LED11	I/O	Connects to the cathode of LED12 and the anode of LED11.
4	LED12	I/O	Connected to GND with a 10nF capacitor. Connects to the anode of LED12.
5	CPP4	O	Output of charge pump. Bypassed to LED12 pin with a ceramic capacitor of at least 0.1μF.
6,31,37,43	NC	NC	-
7,16,30	GND	G	Ground. All GND and NGND pins must be connected.
8,29	SYNC	I/O	Synchronization pin, allowed empty when not in use.. Multiple GALT61120 devices on the same network can be synchronized. The devices can be programmed via a serial interface to provide synchronization pulses, or they can be driven by an MCU unit. Only one device can drive this signal. The drive strength of SYNC is determined by the voltage on the DSTR pin.
9,28	RX	I/O	Receive data pin. Connects the RX pin of the first device to the TX output of the MCU, and connect the other RX pin to the RX pin of the second device. Other devices route to the RX line through both RX pins.
10,27	TX	I/O	Transmit data pin. Connect the TX pin of the first device to the RX input of the MCU, and connect the other TX pin to the TX pin of the second device. Other devices route to the TX line through both TX pins. The driving strength of TX is determined by the voltage on the DSTR pin.
11,26	CLK	I/O	System clock, the primary clock of the device. The clock source can be an external clock or a clock signal generated by a crystal connected to XTALI/XTALO. The drive strength of CLK is determined by the voltage on the DSTR pin and can even be disabled.
12	XTALI	I	Input of the Pierce crystal oscillator inverter. Connect to GND when not in use.

E-TQFP	Name	Type	Function
			Connect to an external crystal oscillator circuit. Can be used to buffer externally generated clocks.
13	XTALO	O	Output of the Pierce crystal oscillator inverter. Connect to an external crystal oscillator circuit. The drive strength of XTALO can be adjusted.
14	VIN	I	Input voltage. Bypassed to GND with a ceramic capacitor of at least 0.1μF. If using a 5V input, connect VIN to GND to bypass the internal regulator.
15	ADC2	AI	ADC input, range: GND ~ VDD. The conversion result comes from the register at address A1h.
17	ADC1	AI	ADC input, range: GND ~ VDD. The conversion result comes from the register at address A0h.
18	DSTR	I	Set drive strength. Bypassed to GND with a ceramic capacitor of up to 10nF. Connect a resistor voltage divider between VDD, GND, and STR to adjust the drive strength of CLK, TX, and SYNC signals, or to disable CLK output.
19	ADDR0	AI	Equal to the least significant bit (LSB) of the device address. The pin function is set to digital input by default. Connect a resistor voltage divider between VDD, GND, and ADDR0 to determine the LSBs of the UART address. If there are 8 or fewer chips on the bus, it can be connected to VDD (logic 1) or GND (logic 0).
20	ADDR1	AI	Equal to the most significant bit (MSB) minus 1 of the device address. Connect to VDD (logic 1) or GND (logic 0).
21	ADDR2	AI	Equal to the most significant bit (MSB) of the device address. Connect to VDD (logic 1) or GND (logic 0).
22	VDD	O	Output of on-chip 5V LDO. Connect two ceramic output capacitors to DGND, with the capacitors placed as close to the pins as possible. Recommended capacitors are 0.1μF (0603 package) and 10nF (0402 package).
23	DGND	G	Digital ground. All GND and NGND pins must be connected.
24	SCL	O	I2C clock line. If using EEPROM, connect a 10KΩ pull-up resistor to VDD; otherwise, refer to the faultsafe mode at power-up.
25	SDA	I/O	I2C data line. If using EEPROM, connect a 10KΩ pull-up resistor to VDD; otherwise, refer to the fault-safe mode at power-up.
32	LED1K	I/O	Connects to the cathode of LED1.
33	LED1A	I/O	Connects to the cathode of LED2 and the anode of LED1.
34	LED2	I/O	Connects to the cathode of LED3 and the anode of LED2.
35	LED3	I/O	Connects to the anode of LED3. Connected to GND with a 10nF capacitor.

E-TQFP	Name	Type	Function
36	CPP1	O	Output of charge pump. Bypassed to LED3 pin with a ceramic capacitor of at least 0.1μF.
38	LED4K	I/O	Connects to the cathode of LED4.
39	LED4A	I/O	Connects to the cathode of LED5 and the anode of LED4.
40	LED5	I/O	Connects to the cathode of LED6 and the anode of LED5.
41	LED6	I/O	Connects to the anode of LED6. Connected to GND with a 10nF capacitor.
42	CPP2	O	Output of charge pump. Bypassed to LED6 pin with a ceramic capacitor of at least 0.1μF.
44	LED7K	I/O	Connects to the cathode of LED7.
45	LED7A	I/O	Connects to the cathode of LED8 and the anode of LED7.
46	LED8	I/O	Connects to the cathode of LED9 and the anode of LED8.
47	LED9	I/O	Connects to the anode of LED9. Connected to GND with a 10nF capacitor.
48	CPP3	O	Output of charge pump. Bypassed to LED9 pin with a ceramic capacitor of at least 0.1μF.

4 Application Examples

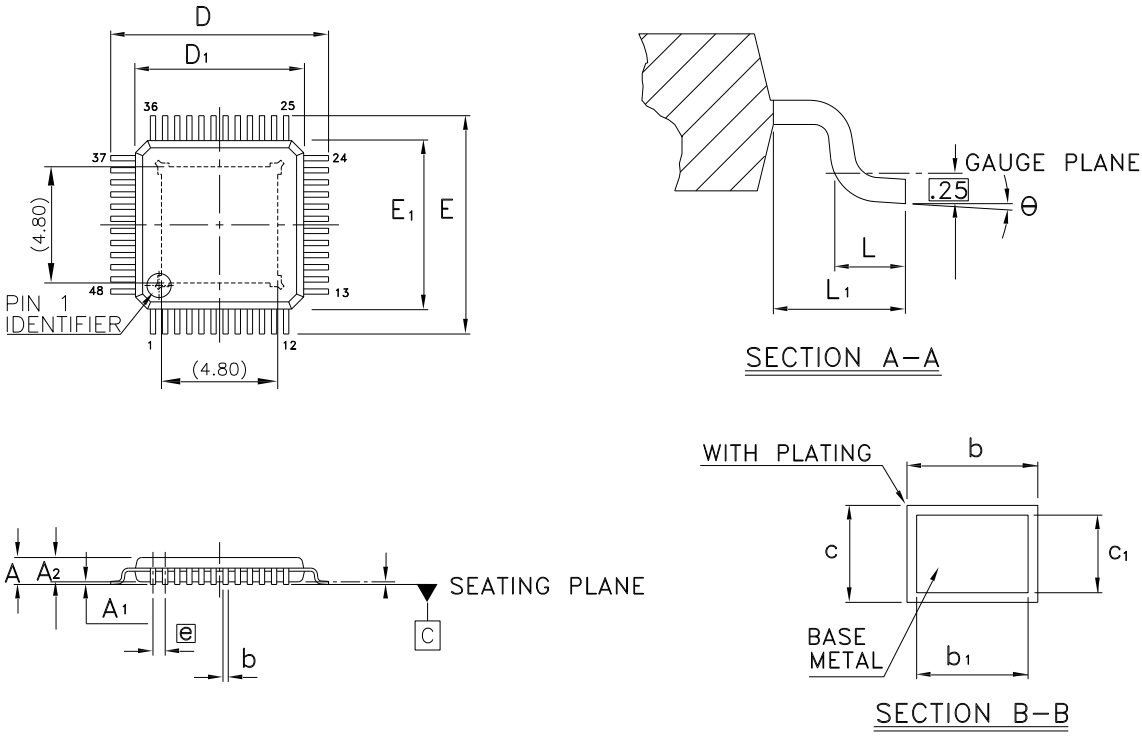
Figure 2 GALT61120 Application Examples



5 Package Information

5.1 E-TQFP48 package information

Figure 3 E-TQFP48 Package Diagram



(1) The figure is not drawn to scale.

(2) All pins should be soldered to the PCB.

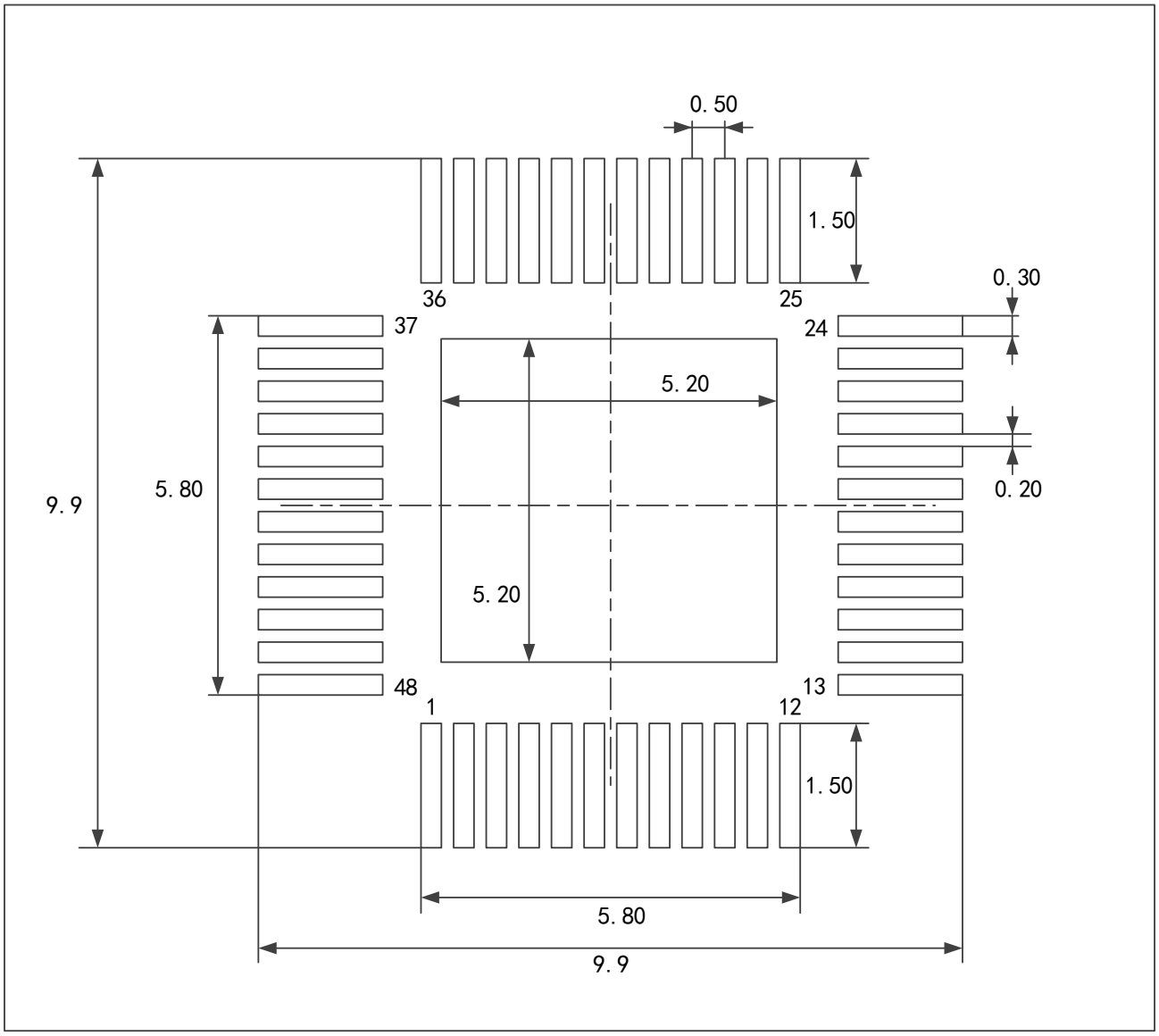
Table 3 E-TQFP48 Package Data.

SYM	Dimensions in mm		
	Min	Nom	Max
A	-	-	1.20
A1	0.025	-	0.127
A2	0.95	1.00	1.05
b	0.17	0.22	0.27
b1	0.17	0.20	0.23
c	0.09	0.14	0.20
c1	0.09	0.12	0.16
D	8.85	9.00	9.15
D1	6.90	7.00	7.10

SYM	Dimensions in mm		
	Min	Nom	Max
E	8.85	9.00	9.15
E1	6.90	7.00	7.10
L	0.45	0.60	0.75
L1	1.00 REF		
e	0.50 BSC		
θ	0°	3.5°	7°

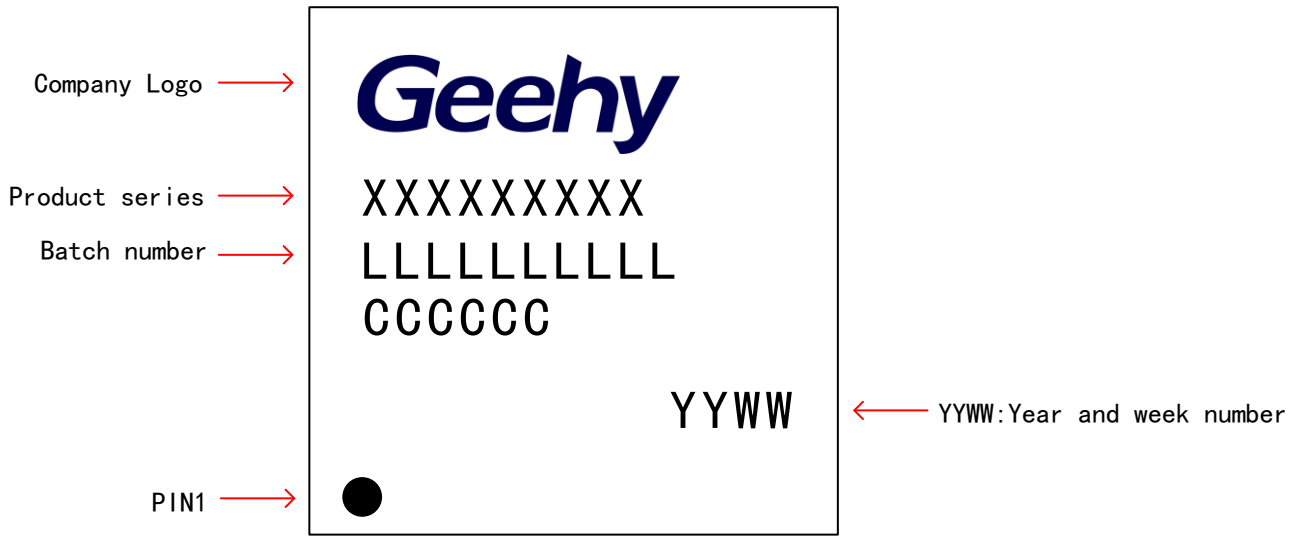
Note: Dimensions are marked in millimeters.

Figure 4 E-TQFP48 Welding Layout Recommendations



Note: Dimensions are marked in millimeters.

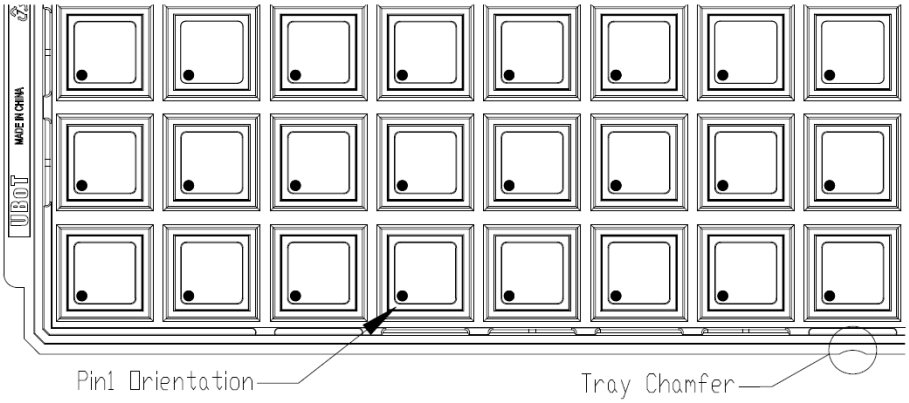
Figure 5 E-TQFP48-48Pins, 7mm x 7mm Schematic Diagram



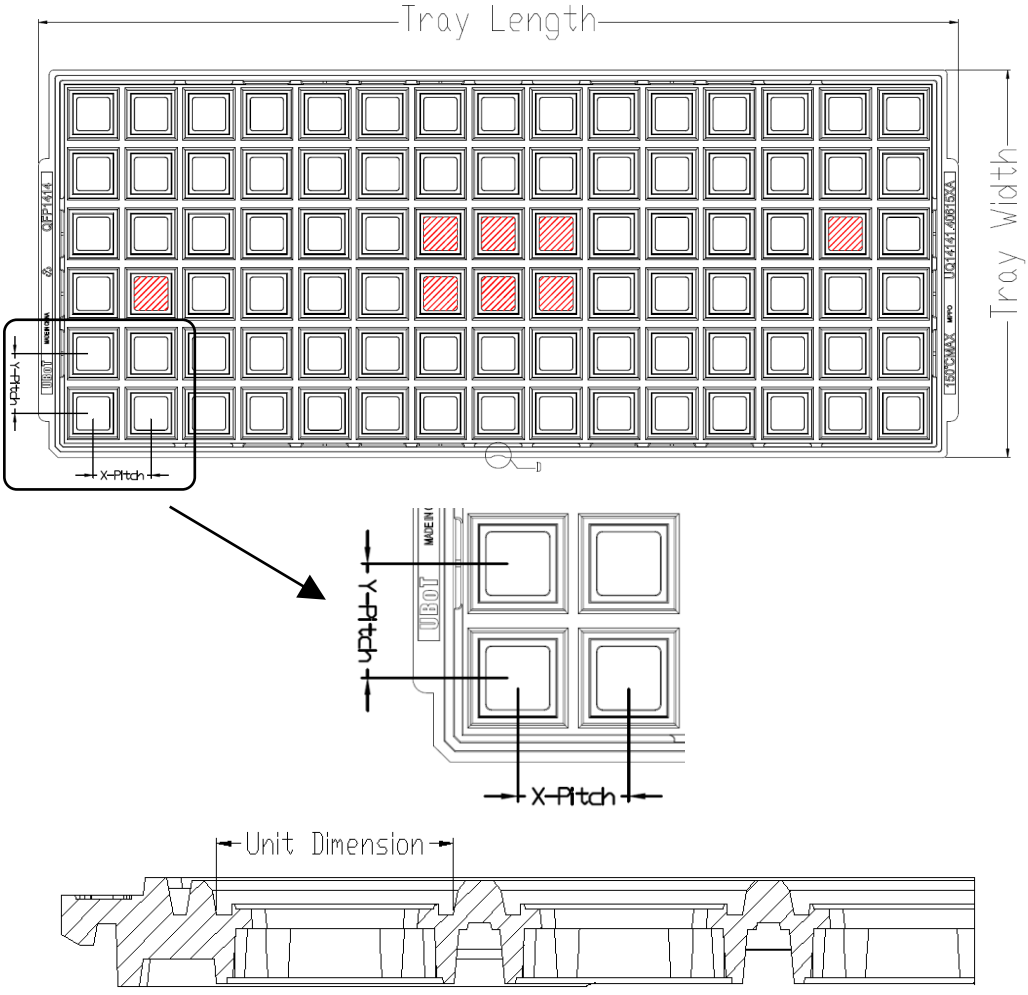
6 Packaging Information

6.1 Tray packaging

Figure 6 Tray Packaging Diagram



Tray Dimensions



All photos are for reference only, and the appearance is subject to the product

Table 4 Tray Packaging Parameter Specification

Device	Package Type	Pins	SPQ	X-Dimension (mm)	Y-Dimension (mm)	X-Pitch (mm)	Y-Pitch (mm)	Tray Length (mm)	Tray Width (mm)
GALT61120	LQFP	48	2500	9.7	9.7	12.2	12.6	322.6	135.9

7 Ordering Information

Figure 7 GALT61120 Product Ordering Information Diagram

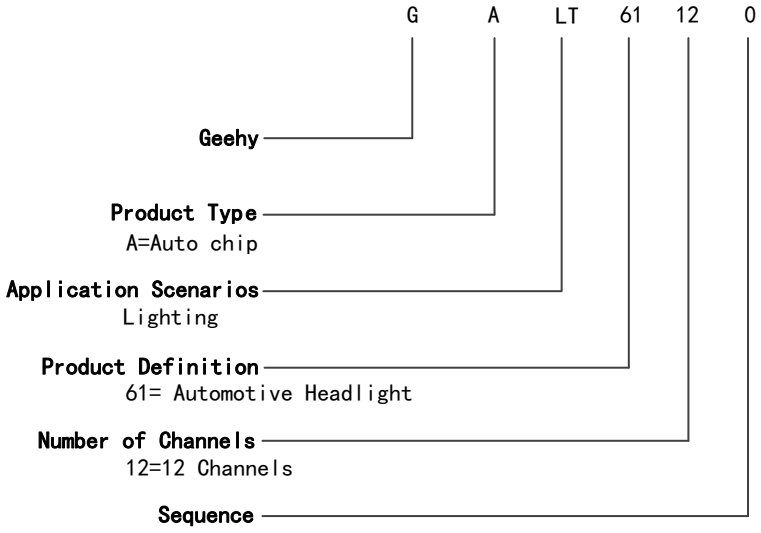


Table 5 Ordering Information Table

Order code	Number of channels	Package	Packaging	SPQ	Range of temperature
GALT61120	12	E-TQFP48	Tray	2500	-40℃~125℃

Note: SPQ=Smallest Packaging Quantity.

8 Commonly Used Function Module Denomination

Table 6 Commonly Used Function Module Denomination

Full name	Abbreviations
Analog-to-digital converter	ADC
Controller local area network	CAN
I2C Interface	I2C
Universal asynchronous transmitter receiver	UART
Universal synchronous and asynchronous transmitter receiver	USART

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